

Product Overview

NSI6602V is a family of high reliability isolated dual-channel gate driver ICs which can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. Each output could source 6A and sink 8A peak current with fast 33ns propagation delay and 6ns maximum delay matching. It is designed to drive power MOSFET, SiC, GaN, and IGBT transistors.

The NSI6602V provides 3000Vrms isolation in SOP16 or SOP14 package, and 5700Vrms isolation in SOW16 or SOW14 package. System robustness is supported by 150kV/us typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 3V to 18V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Key Features

- Isolated dual channel driver
- Input side supply voltage: 3V to 18V
- Driver side supply voltage: up to 25V with UVLO
- 6A peak source and 8A peak sink output
- High CMTI: $\pm 150\text{kV/us}$ typical
- 33ns typical propagation delay
- 6ns maximum delay matching
- 9ns maximum pulse width distortion
- Programmable deadtime
- Accepts minimum input pulse width 20ns
- Operation temperature: $-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$
- AEC-Q100 (Grade 1) qualified for auto-motive Application
- RoHS & REACH Compliance

Safety Regulatory Approvals

- UL recognition:
 - SOW6/SOW14: 5700V_{rms} for 1 minute per UL1577
 - SOP16/SOP14: 3000V_{rms} for 1 minute per UL1577
- DIN EN IEC 60747-17 (VDE 0884-17)
- CSA component notice 5A
- CQC certification per GB4943.

Applications

- Isolated DC-DC and AC-to-DC power supplies in server, telecom, and industry
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Functional Block Diagram

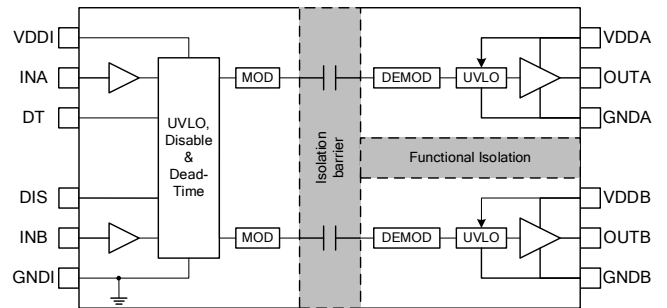


Figure 0.1 NSI6602V Block Diagram

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1. Pin Configuration and Functions

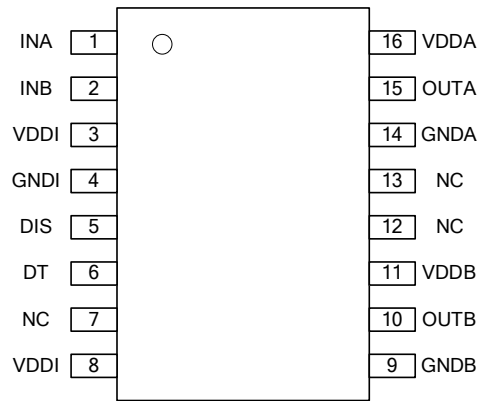


Figure 1.1 NSI6602V SOW16/ SOP16 Package

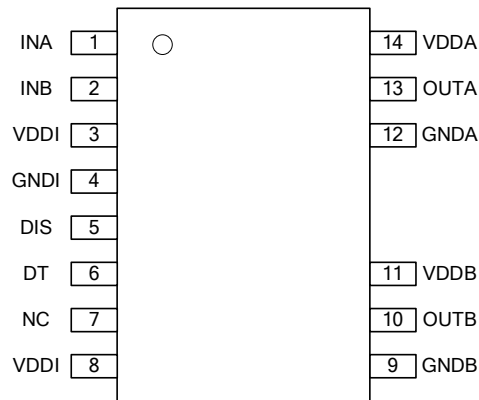


Figure 1.2 NSI6602V SOW14/SOP14 Package

Table 1.1 NSI6602V Pin Configuration and Description

PIN NO.				SYMBOL	FUNCTION
SOW16	SOP16	SOP14	SOW14		
4	4	4	4	GNDI	Input-side ground reference.
1	1	1	1	INA	TTL compatible input signal for channel A with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.
2	2	2	2	INB	TTL compatible input signal for channel B with internal pull down to GNDI. It is recommended to connect this pin to GNDI if not used.
3, 8	3, 8	3, 8	3, 8	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GNDI as close as possible.
5	5	5	5	DIS	Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GNDI if not used.
6	6	6	6	DT	Programmable deadtime control. To allow the outputs overlapping by connecting DT to VDDI. Place a 1kΩ to 200kΩ resistor (RDT) between DT and GNDI to adjust deadtime following: $t_{DT} (ns) = 10 \times RDT (k\Omega)$. It is recommended to parallel a low ESR capacitor, e.g., 2.2nF or above.
9	9	9	9	GNDB	Ground for output channel B
10	10	10	10	OUTB	Output gate driver for channel B
11	11	11	11	VDDB	Supply voltage for channel B
14	14	12	12	GND A	Ground for output channel A
15	15	13	13	OUTA	Output gate driver for channel A
16	16	14	14	VDDA	Supply voltage for channel A
7,12,13	7,12,13	7	7	NC	Not connected

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	-0.3	24	V
Output Side Supply Voltage	VDDA to GND A, VDDB to GNDB	-0.3	30	V
Input Signal Voltage	INA, INB, DIS, DT to GNDI	-0.3	$V_{VDDI}+0.3$	V
	INA, INB, DIS, DT to GNDI, Transient for 50ns	-5	$V_{VDDI}+0.3$	V
Output Signal Voltage	OUTA to GND A, OUTB to GNDB	-0.3	$V_{VDDA}+0.3$ $V_{VDDB}+0.3$	V
	OUTA to GND A, OUTB to GNDB, Transient for 200ns	-2	$V_{VDDA}+0.3$ $V_{VDDB}+0.3$	V

Parameters	Symbol	Min	Max	Unit
Channel A to Channel B Voltage	GNDA to GNDB in SOP16&SOW16 package		1500	V
	GNDA to GNDB in SOW14/SOP14 package		1850	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD RATINGS

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD <ul style="list-style-type: none"> All pins 	±3000	V
	Charged device model (CDM), per AEC-Q100-011-RevB <ul style="list-style-type: none"> All pins 	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	3	18	V
Driver Side Supply Voltage	VDDA to GNDA, VDDB to GNDB	V_{VDDA_ON} , V_{VDDB_ON}	25	V
Input Signal Voltage	INA, INB, DIS, DT	0	V_{VDDI}	V
Ambient Temperature	T_a	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOW16/SOW14	SOP16	Unit
Junction-to-ambient thermal resistance ¹⁾	R_{JA}	97.0	150.5	°C/W
Junction-to-case(top) thermal resistance ²⁾	$R_{JC (top)}$	23.3	21.2	°C/W
Junction-to-top characterization parameter ³⁾	Ψ_{JT}	35.8	52.3	°C/W
Junction-to-board characterization parameter ³⁾	Ψ_{JB}	39.0	55.6	°C/W

- Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
- Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
- Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDDB=15V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I _{VDDIQ}		1.0	2	mA	INA=0, INB=0
VDDI Operating Current	I _{VDDI}		2	3	mA	Input frequency 500kHz
VDDI UVLO Rising Threshold	V _{VDDI_ON}	2.5	2.7	2.9	V	
VDDI UVLO Falling Threshold	V _{VDDI_OFF}	2.3	2.5	2.7	V	
VDDI UVLO Hysteresis	V _{VDDI_HYS}		0.2		V	
Output Side Supply						
VDDA/B Quiescent Current, per Channel	I _{VDDAQ} , I _{VDDBQ}		1	2	mA	INA=0, INB=0
VDDA/B Operation Current, per Channel	I _{VDDA} , I _{VDDDB}		3	4.5	mA	100pF, 500kHz, VDDx=15V
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	5.7	6.15	6.5	V	NSI6602VA (6V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	5.4	5.85	6.2	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		0.3		V	
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	8.1	8.5	8.9	V	NSI6602VB (8V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	7.6	8.0	8.4	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	12.7	13.2	13.7	V	NSI6602VC (12V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	11.7	12.2	12.7	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		1		V	
VDDA/B UVLO Rising Threshold	V _{VDDA_ON} , V _{VDDDB_ON}	3.9	4.2	4.4	V	NSI6602VD (4V)
VDDA/B UVLO Falling Threshold	V _{VDDA_OFF} , V _{VDDDB_OFF}	3.5	3.8	4.1	V	
VDDA/B UVLO Hysteresis	V _{VDDA_HYS} , V _{VDDDB_HYS}		0.3		V	
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB	R _{INA_PD} , R _{INB_PD}	80	100	125	kΩ	
Input Pin Pull Down Resistance, DIS (EN)	R _{DIS_PD}	80	100	125	kΩ	
Logic High Input Threshold	V _{INA_H} , V _{INB_H} , V _{DIS_H}	1.5	1.8	2.1	V	
Logic Low Input Threshold	V _{INA_L} , V _{INB_L} , V _{DIS_L}	0.8	1.1	1.4	V	
Input Hysteresis	V _{INA_HYS} , V _{INB_HYS} , V _{DIS_HYS}		0.7		V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Output Side Characteristic						
Logic High Output Voltage	$V_{VDDA}-V_{OUTA_H}$, $V_{VDDB}-V_{OUTB_H}$		0.1		V	$I_{out} = 100mA$
Logic Low Output Voltage	V_{OUTA_L} , V_{OUTB_L}		35		mV	$I_{out} = -100mA$
Output Source Resistance	R_{OUTA_H} , R_{OUTB_H}		1		Ω	$I_{out} = 100mA$
Output Sink Resistance	R_{OUTA_L} , R_{OUTB_L}		0.35		Ω	$I_{out} = -100mA$
Peak Output Source Current	I_{OUTA+} , I_{OUTB+}		6		A	
Peak Output Sink Current	I_{OUTA-} , I_{OUTB-}		8		A	

6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at Ta=25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		15	25	ns	
Propagation Delay	t_{PDHL} , t_{PDLH}		33	45	ns	
Pulse Width Distortion $ t_{PDLH}-t_{PDHL} $	t_{PWD}			9	ns	
Channel to Channel Delay Matching	t_{DMLH} , t_{DMHL}			6	ns	
Programmed Deadtime	t_{DT}	160	200	240	ns	$t_{DT}(ns)=10 \cdot R(k\Omega)$; Test for R = 20k Ω
Output Rise Time (10% to 90%)	t_R		15		ns	CL=1.8nF, VDDx=15V
Output Fall Time (90% to 10%)	t_F		15		ns	CL=1.8nF, VDDx=15V
Shutdown Time from Disable True	t_{DIS}		50	80	ns	
Recovery Time from Disable False	t_{EN}		50	80	ns	
VDDI Power-up Time Delay (Time from VDDI = V_{VDD_ON} to OUTA/B = INA/B)	t_{start_VDDI}		12	25	us	INA or INB tied to VDDI
VDDA/B Power-up Time Delay (Time from VDDA/B = V_{VDD_ON} to OUTA/B = INA/B)	t_{start_VDDA} , t_{start_VDDB}		18	26	us	INA or INB tied to VDDI $C_{OUTA/B}=1.8nF$
Common Mode Transient Immunity	CMTI	100	150		kV/us	verified by design

6.3. Typical Performance Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=15V, TA = 25°C. Output has no load unless otherwise noted.

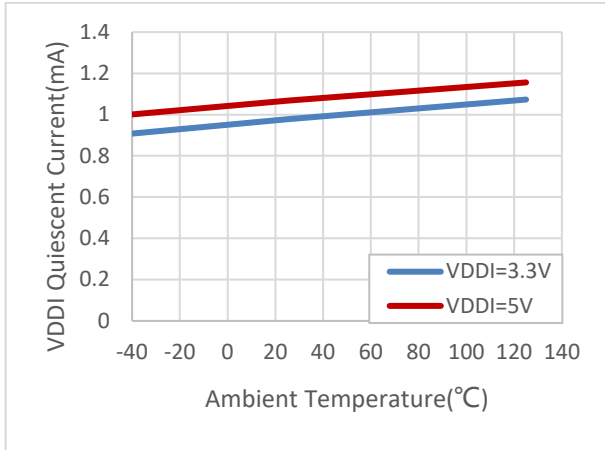


Figure 6.1 VDDI Quiescent Current vs Temperature

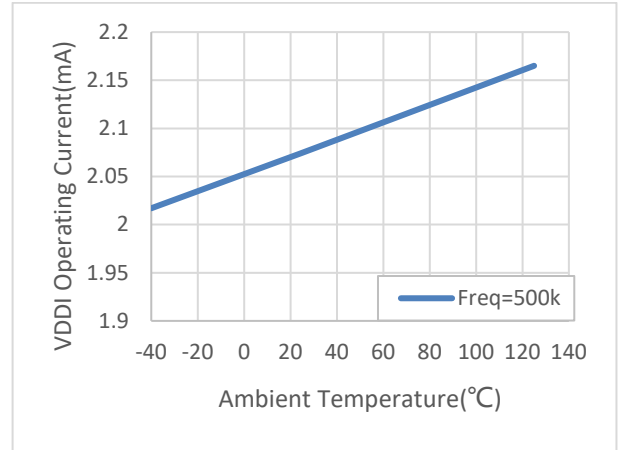


Figure 6.2 VDDI Operating Current vs Temperature

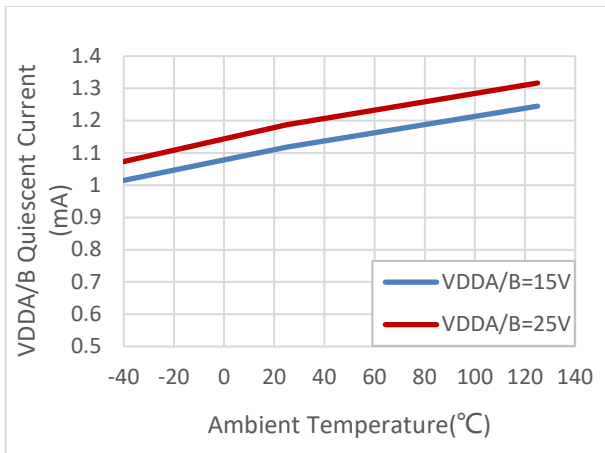


Figure 6.3 VDDA/B Quiescent Current vs Temperature

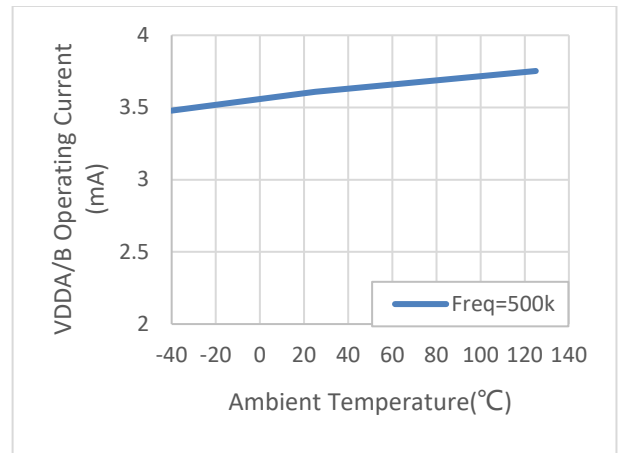


Figure 6.4 VDDA/B Operating Current vs Temperature

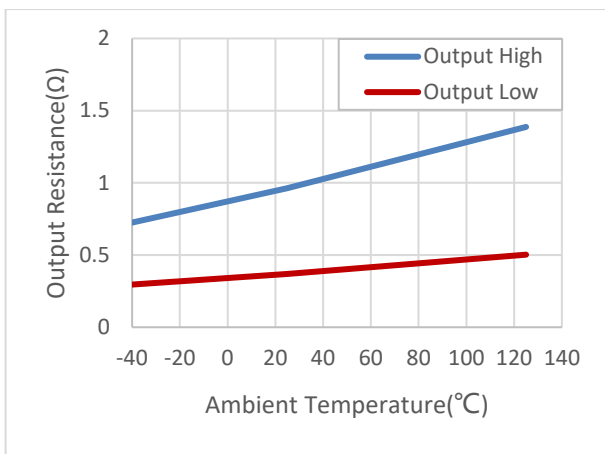


Figure 6.5 Output Resistance vs Temperature

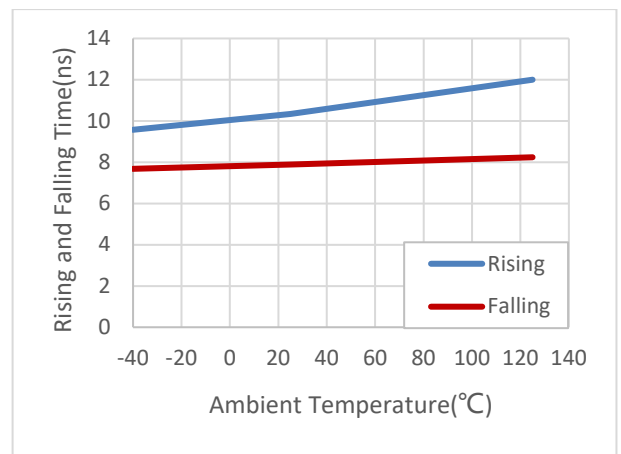


Figure 6.6 Typical Rise Time & Fall Time vs Temperature

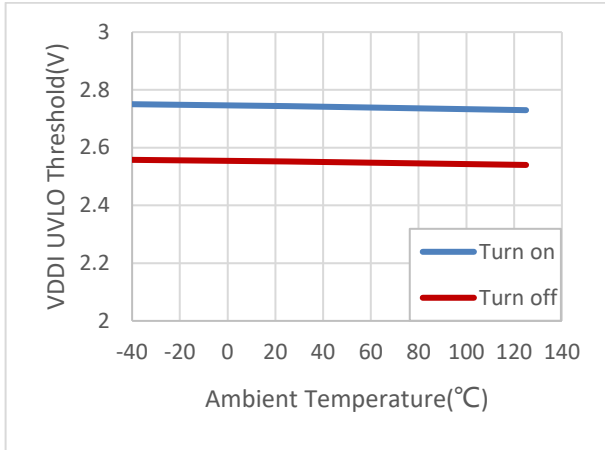


Figure 6.7 VDDI UVLO Threshold vs Temperature

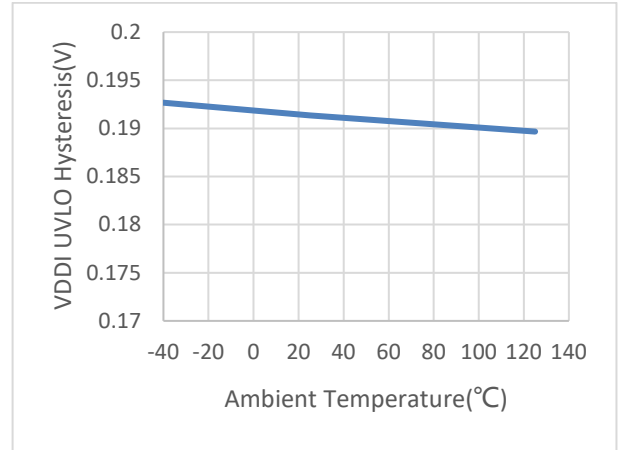


Figure 6.8 VDDI UVLO Hysteresis vs Temperature

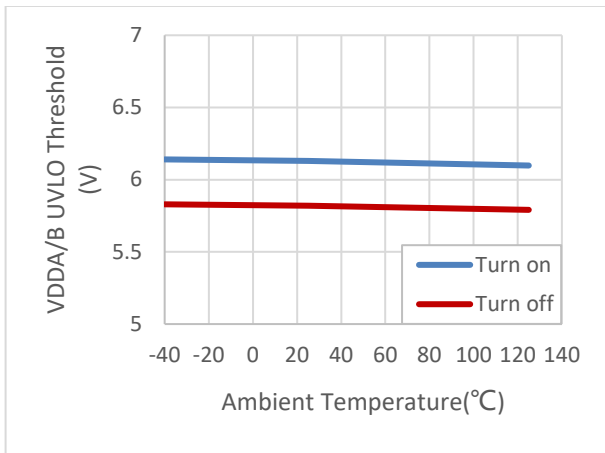


Figure 6.9 6V VDDA/B UVLO Threshold vs Temperature

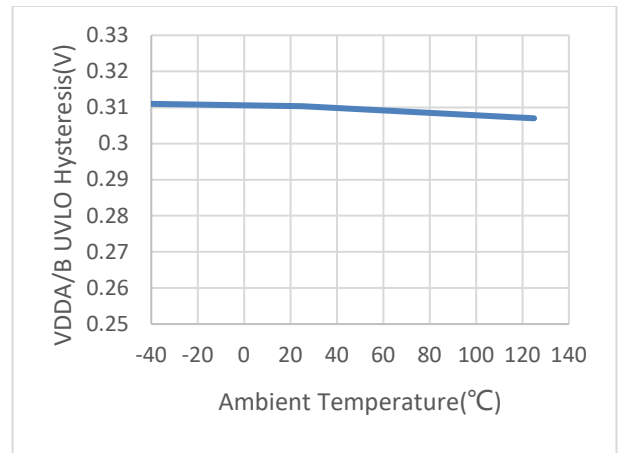


Figure 6.10 6V VDDA/B UVLO Hysteresis vs Temperature

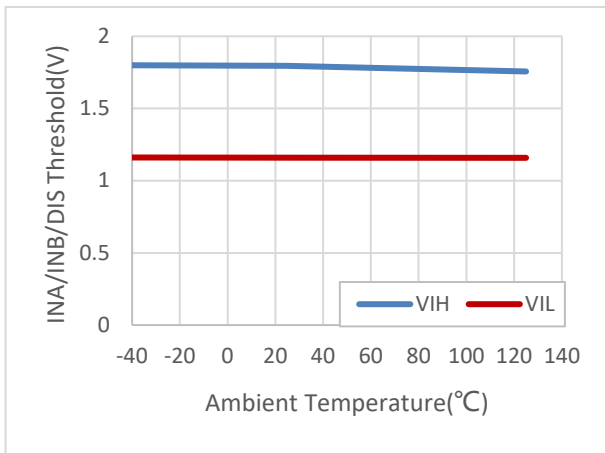


Figure 6.11 INA/INB/DIS Threshold vs Temperature

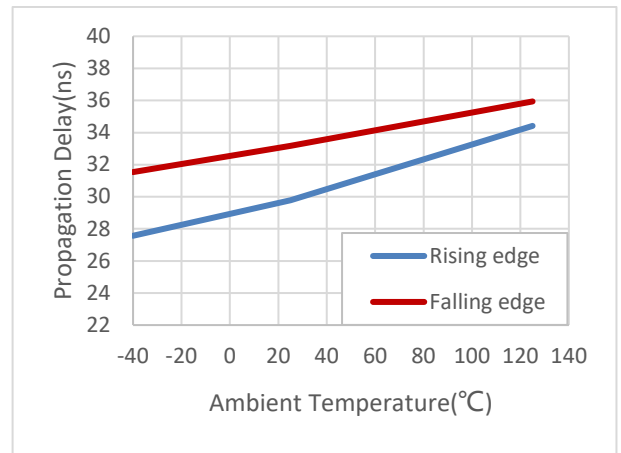


Figure 6.12 Propagation Delay vs Temperature

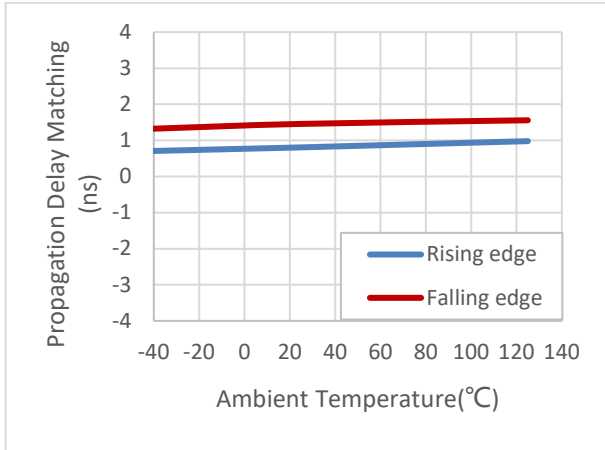


Figure 6.13 Propagation Delay Matching vs Temperature

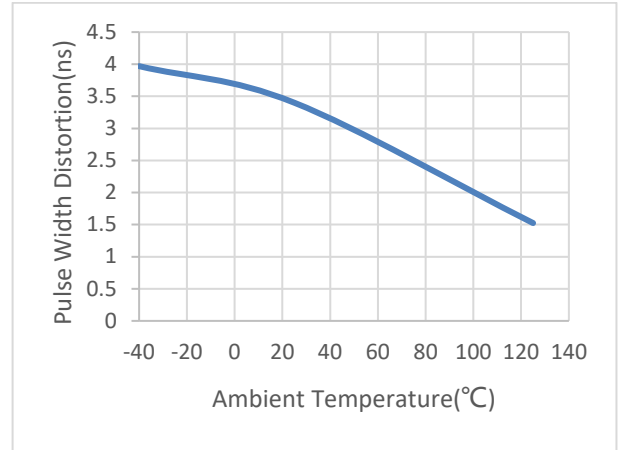


Figure 6.14 Pulse Width Distortion vs Temperature

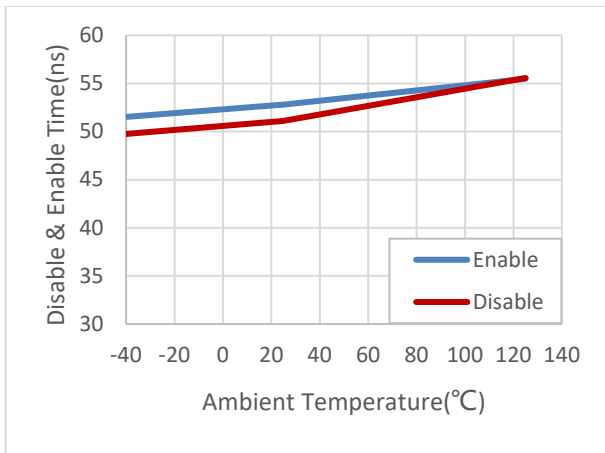


Figure 6.15 Disable & Enable Time vs Temperature

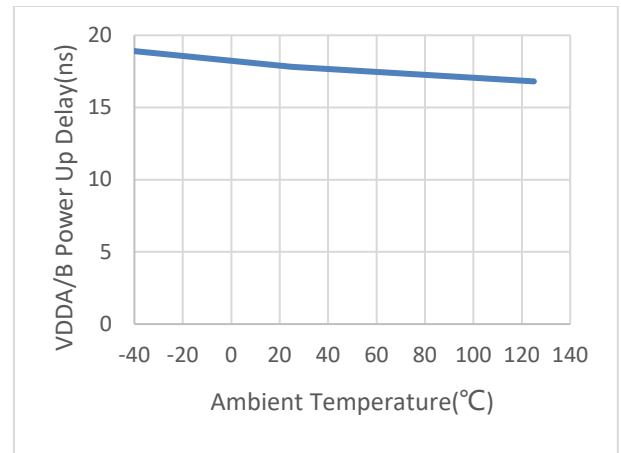


Figure 6.16 VDDA/B power up delay vs Temperature

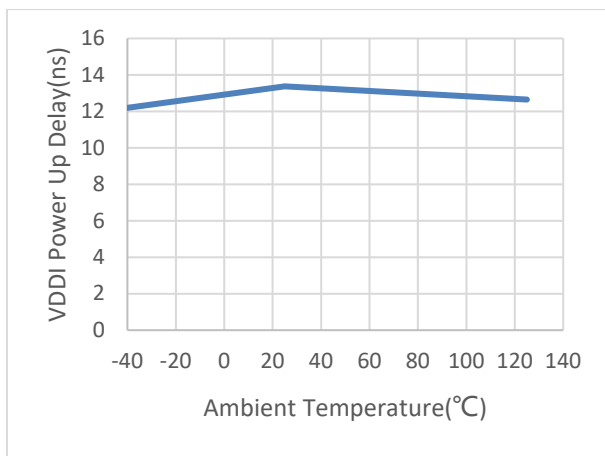


Figure 6.17 VDDI power up delay vs Temperature

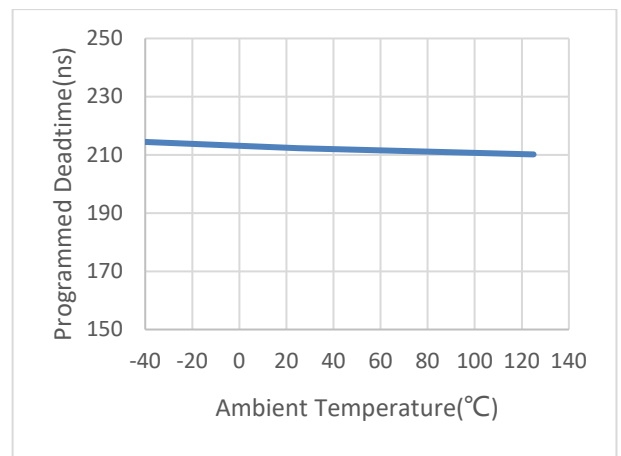


Figure 6.18 Deadtime (RDT=20kΩ) vs Temperature

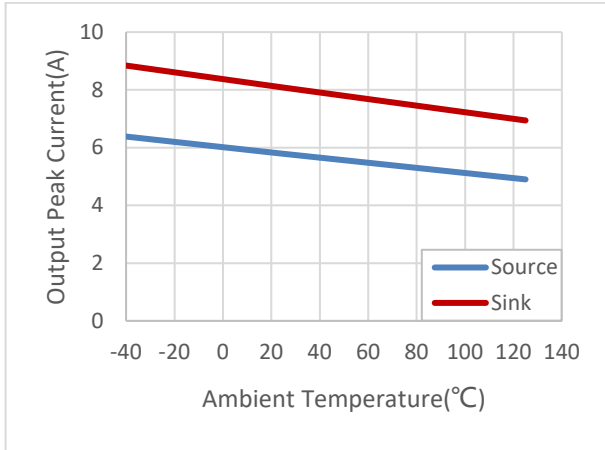


Figure 6.19 Peak current vs Temperature

6.4. Parameter Measurement Information

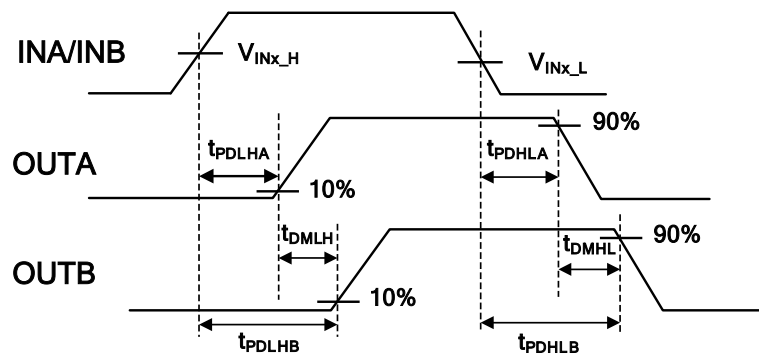


Figure 6.20 Propagation Delay and Channel to Channel Delay Match Time, connect DT to VDDI

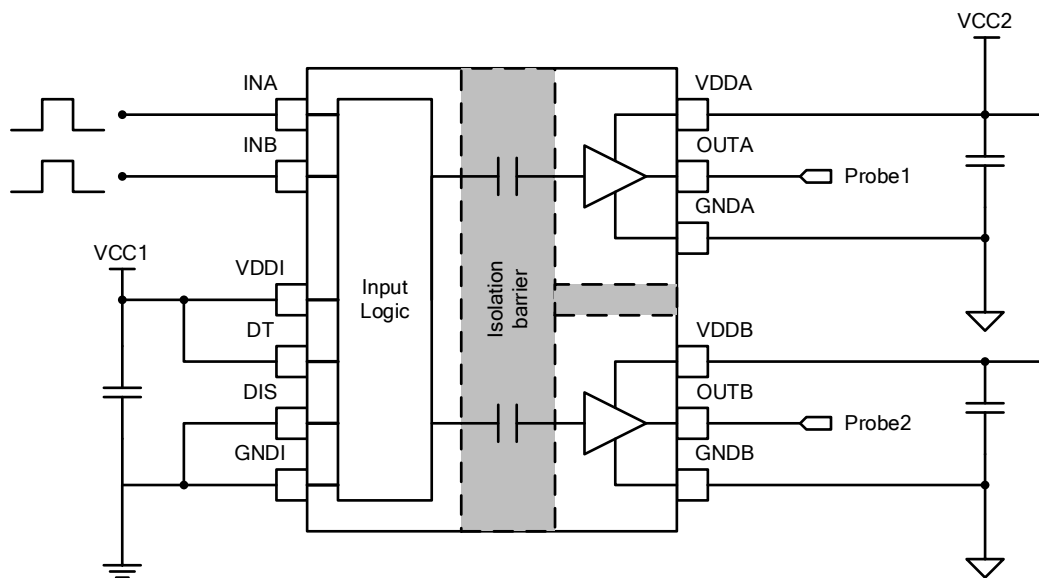


Figure 6.21 Channel to Channel Delay Match Test Circuit

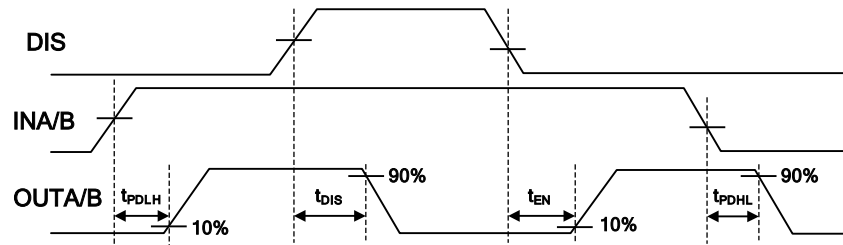


Figure 6.22 Disable Time and Enable Time

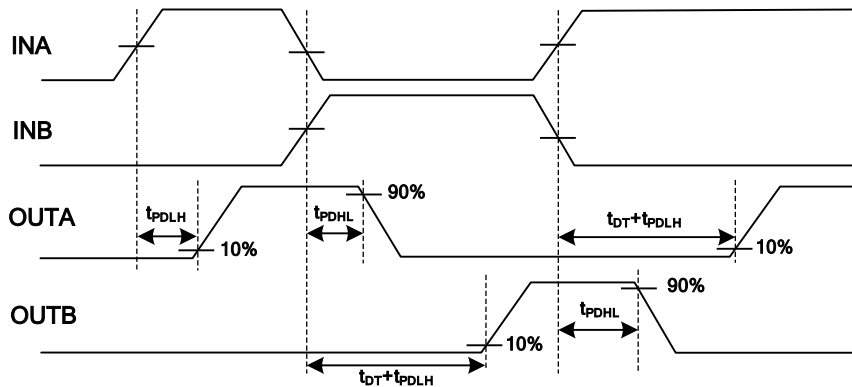


Figure 6.23 Deadtime, Determined by RDT

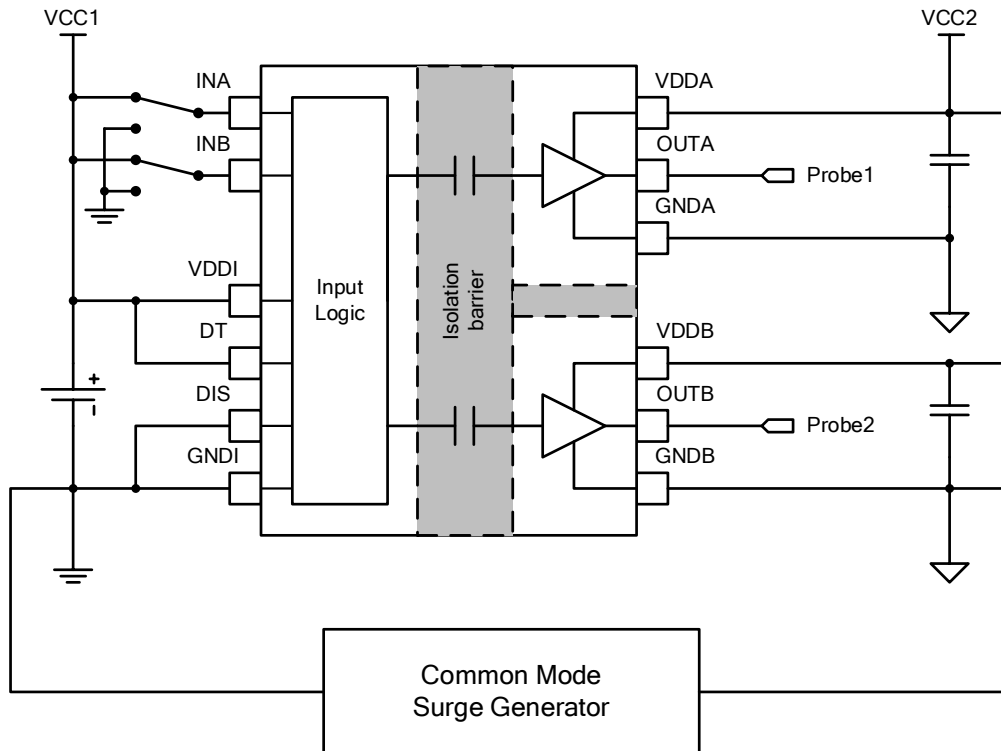


Figure 6.24 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation Characteristics

Description	Test Condition	Symbol	Value		Unit
			SOW16/14	SOP16/14	
Min. External Air Gap (Clearance)		CLR	8	4	mm
Min. External Tracking (Creepage)		CPG	8	4	mm
Distance through the Insulation		DTI	28		um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60664-1		I		
Overvoltage Category per IEC60664-1	For Rated Mains Voltage $\leq 150V_{rms}$		I to IV	I to IV	
	For Rated Mains Voltage $\leq 300V_{rms}$		I to IV	I to III	
	For Rated Mains Voltage $\leq 600V_{rms}$		I to IV	I to II	
	For Rated Mains Voltage $\leq 1000V_{rms}$		I to III	/	
Climatic Category			40/125/21		
Pollution Degree	per DIN VDE 0110, Table 1		2		
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1000	700	V_{RMS}
	DC voltage		1414	990	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60s$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$	q_{pd}	<5	/	pC
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.6*V_{IORM}$, $t_m=10s$			/	pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$, $V_{pd(m)}=1.875*V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)			/	pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, $V_{ini}=V_{IOTM}$, $t_{ini} = 60 s$, $V_{pd(m)}=1.2*V_{IORM}$, $t_m=10s$	q_{pd}	/	<5	pC

Description	Test Condition	Symbol	Value		Unit
	Method a, after environmental tests subgroup 1, $V_{ini}=V_{IOTM}$, $t_{ini}=60s$, $V_{pd(m)}=1.3*V_{IORM}$, $t_m=10s$		/		pC
	Method b, routine test (100% production) and preconditioning (type test); $V_{ini}=1.2*V_{IOTM}$, $t_{ini}=1s$ $V_{pd(m)}=1.5*V_{IORM}$, $t_m=1s$ (method b1) or $V_{pd(m)}=V_{ini}$, $t_m=t_{ini}$ (method b2)		/		pC
Maximum Transient Isolation Voltage	$t = 60 \text{ sec}$	V_{IOTM}	8000	4242	V_{peak}
Maximum impulse voltage	Tested in air, 1.2/50us waveform per IEC62368-1	V_{imp}	6000	3500	V_{peak}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geq V_{IMP} \times 1.3$	V_{IOSM}	10000	6000	V_{peak}
Isolation Resistance	$V_{IO} = 500 \text{ V}$, $T_{amb} = 25^\circ\text{C}$	R_{IO}	$>10^{12}$		Ω
	$V_{IO} = 500 \text{ V}$, $T_{amb} = T_s$		$>10^9$		Ω
	$V_{IO} = 500 \text{ V}$, $100^\circ\text{C} \leq T_{amb} \leq 125^\circ\text{C}$		$>10^{11}$		Ω
Isolation Capacitance	$f = 1\text{MHz}$	C_{IO}	1.2		pF
Insulation Specification per UL1577					
Withstand Isolation Voltage	$V_{TEST} = 1.2 \times V_{ISO}$, $t = 1 \text{ sec}$, 100% production test	V_{ISO}	5700	3000	V_{rms}

7.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI6602Vx-Q1SWxR (SOW16/SOW14)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA} = 97^\circ\text{C/W}^1$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$	Input	12	mW
		Driver A, Driver B	638	mW
		Total	1288	mW
Safety Supply Current	$R_{\theta JA} = 97^\circ\text{C/W}^1$, $V_{DDA/B} = 12\text{V}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$	Driver A, Driver B	53.1	mA
	$R_{\theta JA} = 97^\circ\text{C/W}^1$, $V_{DDA/B} = 25\text{V}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$	Driver A, Driver B	25.5	mA
Safety Temperature ²⁾			150	$^\circ\text{C}$

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW16/SOW14 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

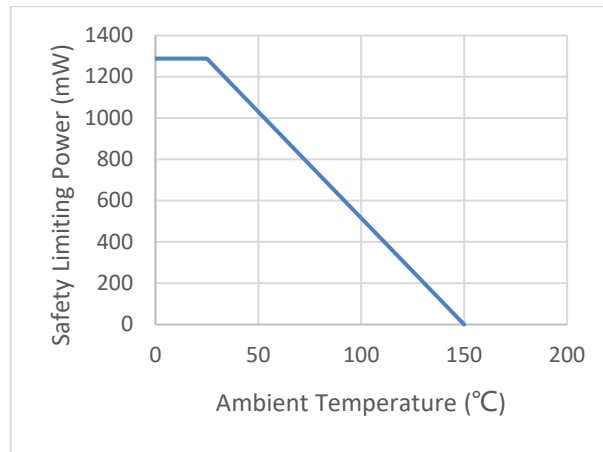


Figure 7.1 NSI6602x-Q1SWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17.

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI6602Vx-xSPxR (SOP16/SOP14)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C}/\text{W}^1$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Input	12	mW
		Driver A, Driver B	409	mW
		Total	830	mW
Safety Supply Current	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C}/\text{W}^1$, $V_{DDA/B} = 12\text{V}$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Driver A, Driver B	34.0	mA
	$R_{\theta JA} = 150.5 \text{ } ^\circ\text{C}/\text{W}^1$, $V_{DDA/B} = 25\text{V}$, $T_J = 150 \text{ } ^\circ\text{C}$, $T_A = 25 \text{ } ^\circ\text{C}$	Driver A, Driver B	16.3	mA
Safety Temperature ²⁾			150	°C

- 1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16/SOP14 package ([Thermal Information Table](#)) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.
- 2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

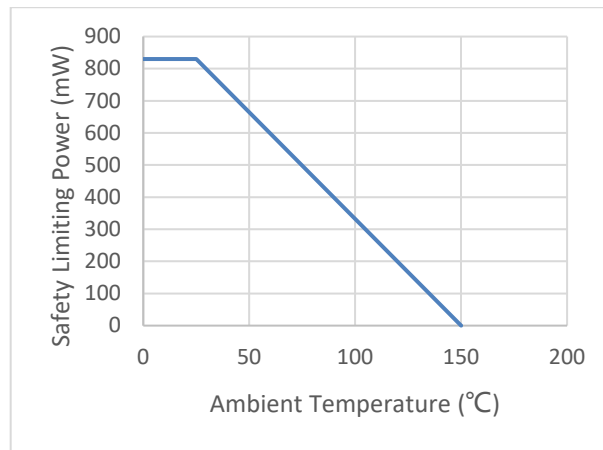


Figure 7.2 NSI6602Vx-Q1SPxR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-17.

7.3. Safety-Related Certifications

The NSI6602Vx-Q1SWxR(SOW16/SOW14) are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1
Single Protection, 5700Vrms Isolation voltage	Single Protection, 5700Vrms Isolation voltage	Reinforced insulation at $V_{IORM}=1414V_{peak}$ $V_{IOSM}=10000V_{peak}$ $V_{IOTM}=8000V_{peak}$	Reinforced insulation
E500602	E500602	40052820	CQC21001289932

The NSI6602Vx-Q1SPNR(SOP16) are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-17	Certified according to GB4943.1
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic insulation at $V_{IORM}=990V_{peak}$ $V_{IOSM}=6000V_{peak}$ $V_{IOTM}=4242V_{peak}$	Basic insulation
E500602	E500602	40057024	CQC21001289932

The NSI6602Vx-Q1SPOR(SOP14) are approved or pending approval by the organizations listed in table.

UL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-17	Certified according to GB4943.1
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic insulation at $V_{IORM}=990V_{peak}$ $V_{IOSM}=6000V_{peak}$ $V_{IOTM}=4242V_{peak}$	Basic insulation
File(pending)	File(pending)	File(pending)	File(pending)

8. Function Description

8.1. Overview

NSI6602V is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI6602V has some useful protections, such as under voltage lock out (UVLO) for both input and output supply, a disable pin, deadtime control, default low output as input is floating. The functional circuit block diagram is shown as below:

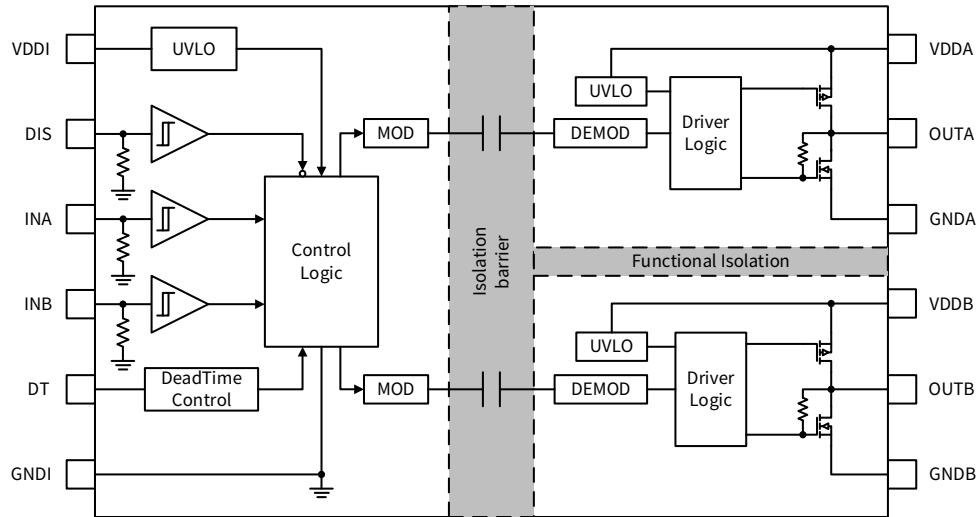


Figure 8.1 Functional Block Diagram

8.2. Under Voltage Lock out (UVLO)

The NSI6602V has an internal under voltage lock out (UVLO) protection on both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis (V_{VDD_HYS}) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

8.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 8.1 Output status vs. Input and Power status

VDDI status	VDDA/B status	DIS	IN		OUT		NOTE ¹⁾
			A	B	A	B	
PU	PU	L or O	L	H	L	H	If Deadtime function is used, output transits to high after the deadtime expires.
PU	PU	L or O	H	L	H	L	
PU	PU	L or O	H	H	H	H	DT pin is pulled to VDDI.
PU	PU	L or O	H	H	L	L	DT is left open or programmed with R _{DT} .
PU	PU	L or O	L	L	L	L	
PU	PU	L or O	O	O	L	L	
PU	PU	H	X	X	L	L	
PU	PD	X	X	X	L	L	
PD	PU	X	X	X	L	L	

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

8.4. Programmable Deadtime (DT pin)

8.4.1. Pulling the DT Pin to VDDI

This allows outputs match inputs completely and no deadtime is asserted.

8.4.2. DT Pin Left Open or Connected to a Programming Resistor between DT and GNDI Pins

If the DT pin is left open, the deadtime duration (t_{DT}) is set to <35ns. t_{DT} can be programmed by placing a resistor, R_{DT}, between the DT pin and GNDI. The appropriate R_{DT} value can be determined from Equation 1, where R_{DT} is in kΩ and t_{DT} in ns:

$$t_{DT} \approx 10 \times R_{DT} \tag{1}$$

The recommended value of R_{DT} is between from 1kΩ to 200kΩ. The steady state voltage at DT pin is about 0.8 V and the DT pin current will be less than 10uA when R_{DT} =100kΩ. It is also recommended to parallel a ceramic capacitor, for example 2.2nF, with R_{DT} to achieve better noise immunity.

The programmed deadtime is activated by the input signal’s falling edge to prevent shoot-through when the device is designed in an application of high side and low side driver. The details of input and output logic with deadtime are shown as Figure 8.2:

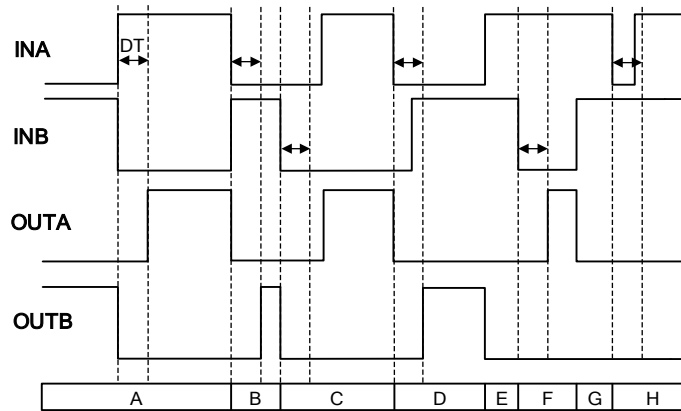


Figure 8.2 Input and Output Logic with the Programmed Deadtime

Condition	Result
A: INA goes high, and INB goes low.	OUTB goes low immediately, then OUTA goes high after the programmed deadtime which is assigned at INB goes low.
B: INA goes low, and INB goes high.	OUTA goes low immediately, then OUTB goes high after the programmed deadtime which is assigned at INA goes low.
C: INB goes low, then INA goes high after deadtime.	OUTB goes low immediately, then OUTA goes high immediately when INA goes high.
D: INA goes low, then INB goes high before deadtime.	OUTA goes low immediately, then OUTB goes high after deadtime
E: INA goes high, INB is still high.	OUTB goes low immediately and OUTA keeps low.
F: INA is still high, INB goes low.	OUTA goes high after deadtime while INB is low and OUTB keeps low.
G: INA is still high, INB goes high after deadtime	OUTA goes low immediately and OUTB keeps low.
H: INA goes low then goes high before deadtime while INB is still high.	OUTA keeps low and OUTB keeps low because deadtime control.

8.5. ESD Protection

Figure 8.3 shows the multiple diodes involved in the ESD protection part of NSI6602V.

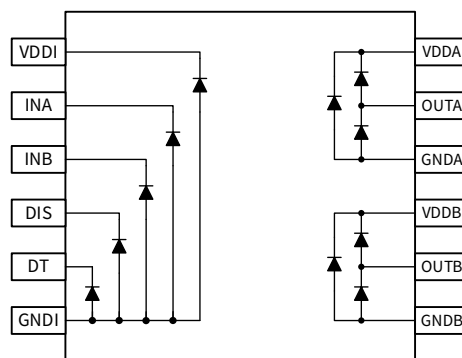


Figure 8.3 ESD Structure

9. Application Note

9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSI6602V which could be used in several popular power converter topologies such as half-bridge/ full bridge/ LLC isolated topologies, buck-boost topologies and 3-phase motor drive applications.

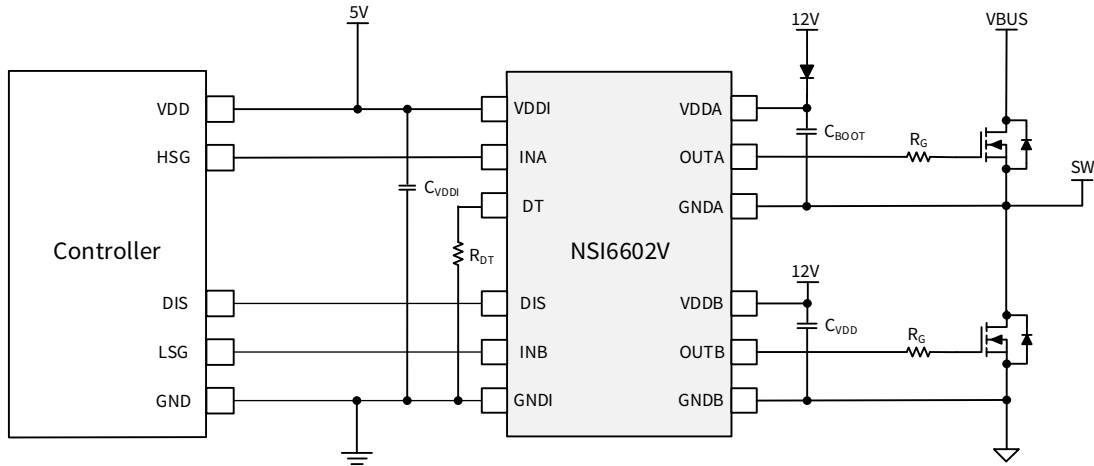


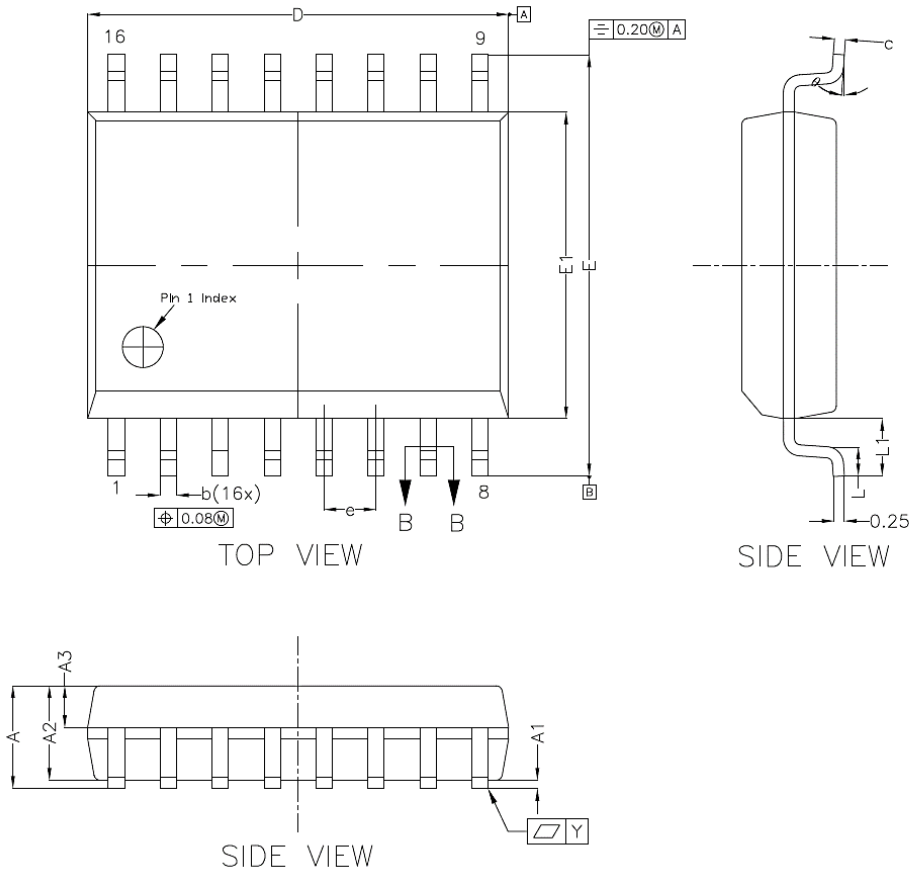
Figure 9.1 Typical Half-Bridge Application Schematic

9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are given as below:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GNDI and pin VDDA/B to GND A/B.
- There is high frequency switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI6602V close to power transistor.
- Large amount of copper should be placed at VDDA/B pin and GND A/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

10. Package information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.1 SOW16 Package Shape and Dimension

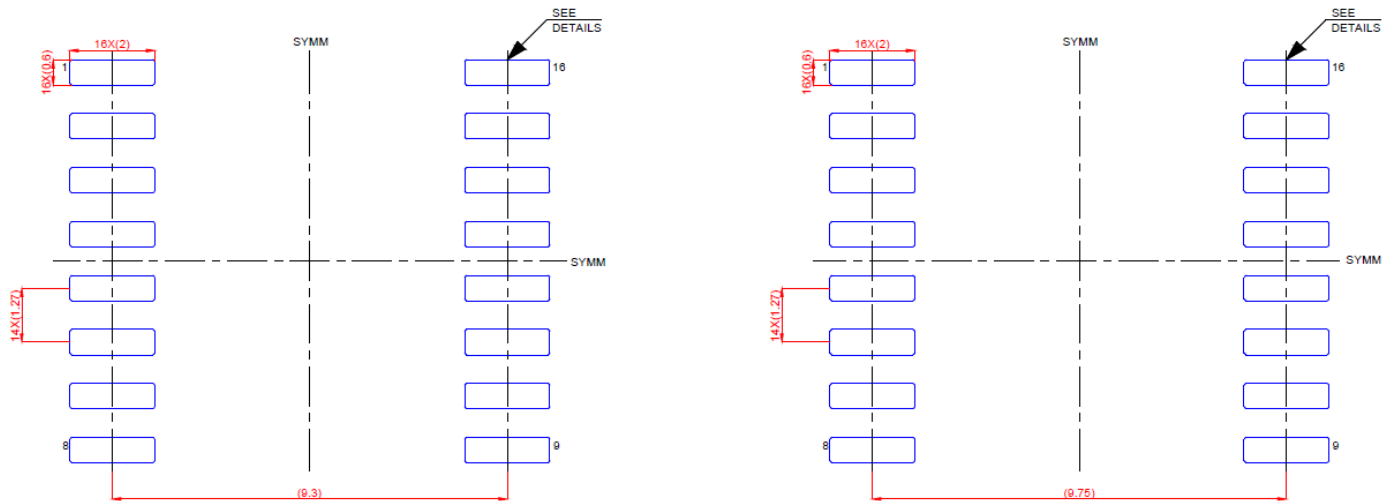
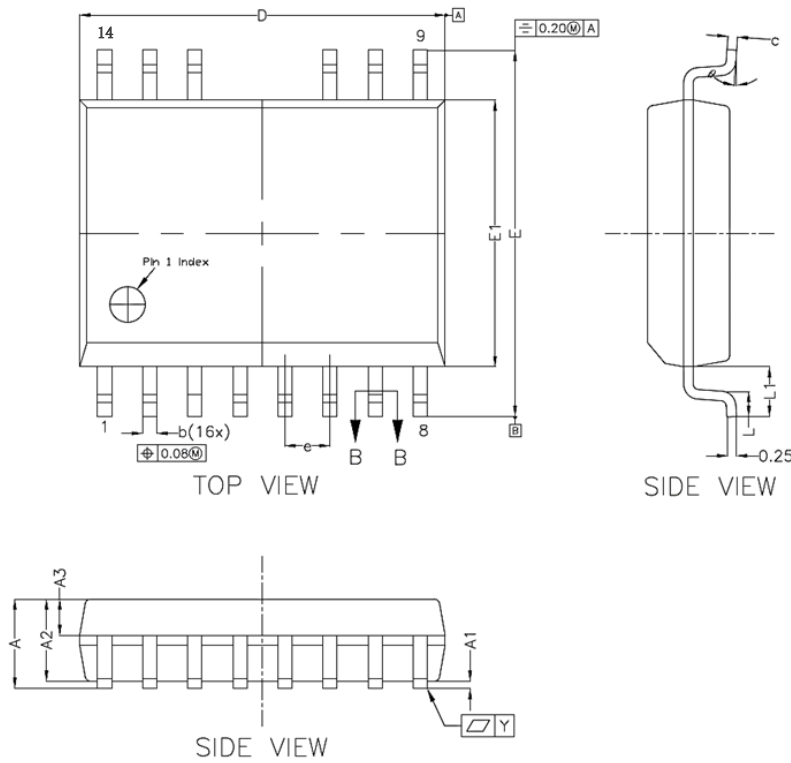


Figure 10.2 SOW16 Package Board Layout Example(mm)



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.3 SOW14 Package Shape and Dimension

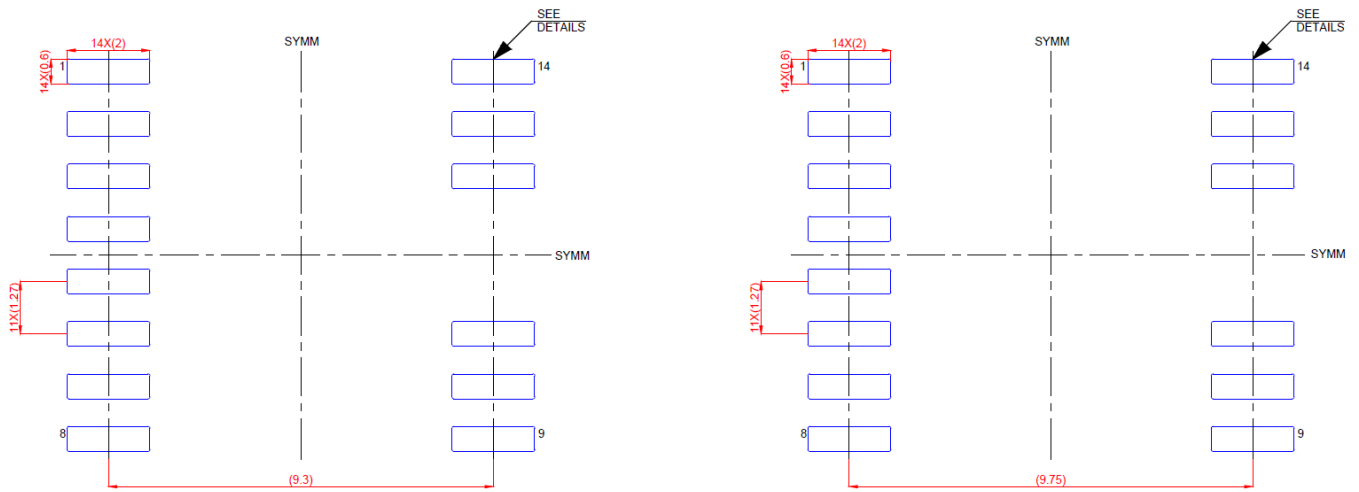
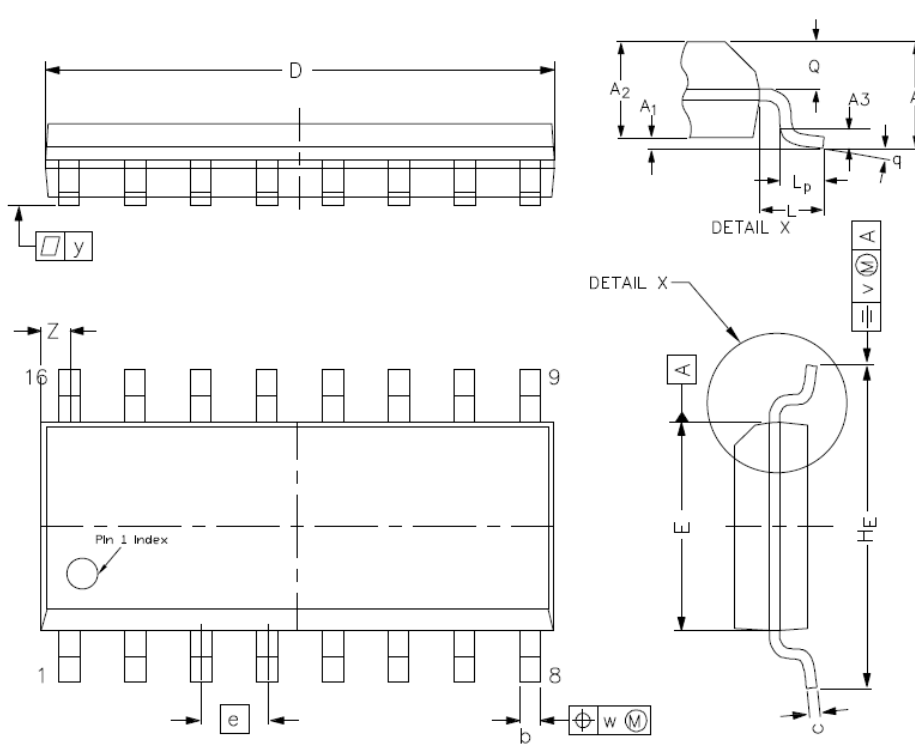


Figure 10.4 SOW14 Package Board Layout Example(mm)



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	----	----	1.75	----	----	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	1.25	----	1.45	0.049	----	0.057
b	0.36	----	0.49	0.014	----	0.019
c	0.19	----	0.25	0.007	----	0.010
D	9.80	9.90	10.0	0.386	0.390	0.394
E	3.80	3.90	4.00	0.150	0.154	0.158
HE	5.80	----	6.20	0.228	----	0.244
Q	0.60	----	0.70	0.024	----	0.028
e	1.27 bsc		0.050 bsc			
L	1.05 bsc		0.041 bsc			
Lp	0.40	----	1.00	0.016	----	0.039
Y	----	0.10	----	----	0.004	----
A3	----	0.25	----	----	0.010	----
Z	0.30	----	0.70	0.012	----	0.028
θ	0°	----	8°	0°	----	8°

Figure 10.5 SOP16 Package Shape and Dimension

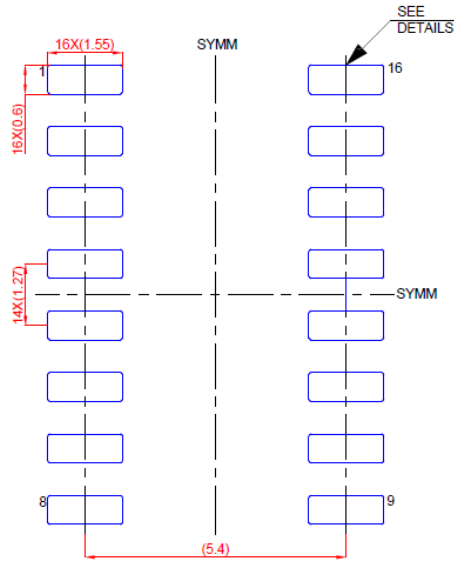


Figure 10.6 SOP16 Package Board Layout Example (mm)

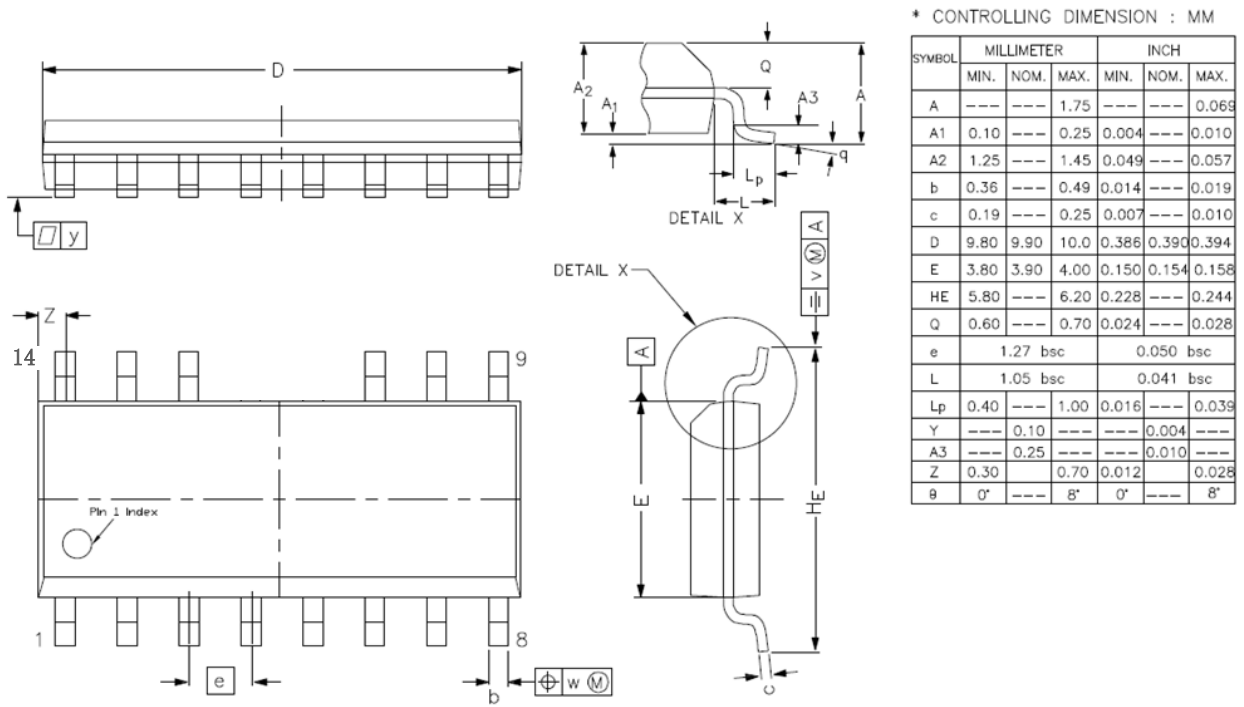


Figure 10.7 SOP14 Package Shape and Dimension

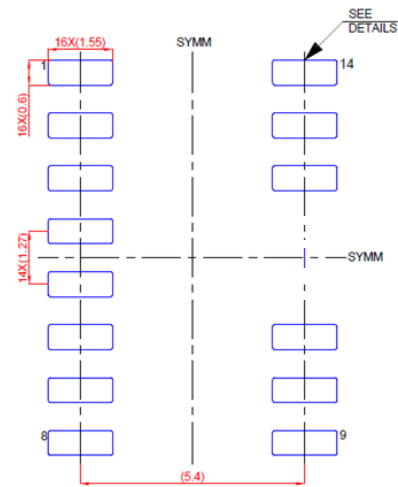


Figure 10.8 SOP14 Package Board Layout Example(mm)

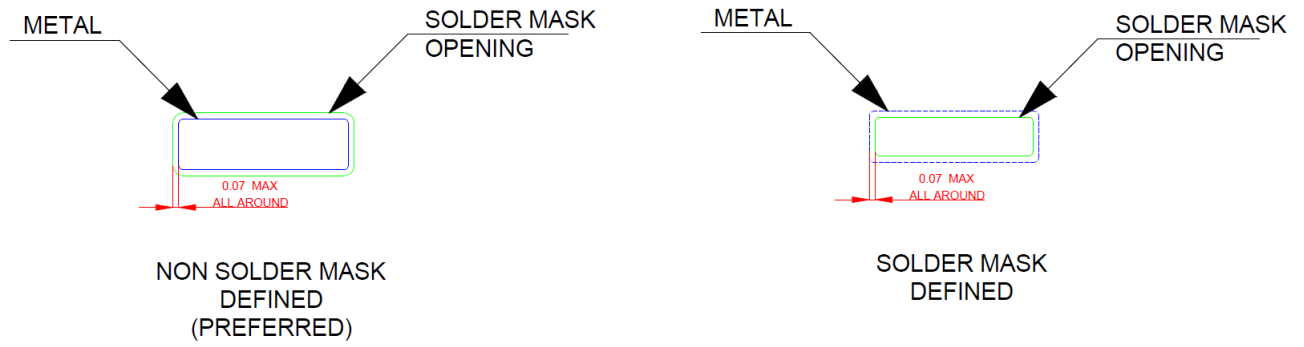


Figure 10.9 Solder Mask Details(mm)

11. Ordering Information

Part No.	Isolation Rating(kV_{RMS})	Driver-side UVLO TYP.	Temperature	Auto-motive	Body Size (mm)	Package	MSL	SPQ
NSI6602VA-Q1SWR	5.7	6V	-40 to 125°C	YES	10.3X7.5X2.65	SOW16	2	1000
NSI6602VA-Q1SWKR	5.7	6V	-40 to 125°C	YES	10.3X7.5X2.65	SOW14	2	1000
NSI6602VA-Q1SPNR	3.0	6V	-40 to 125°C	YES	9.9X3.9X1.75	SOP16	2	2500
NSI6602VA-Q1SPOR	3.0	6V	-40 to 125°C	YES	9.9X3.9X1.75	SOP14	2	2500
NSI6602VB-Q1SWR	5.7	8V	-40 to 125°C	YES	10.3X7.5X2.65	SOW16	2	1000
NSI6602VB-Q1SWKR	5.7	8V	-40 to 125°C	YES	10.3X7.5X2.65	SOW14	2	1000
NSI6602VB-Q1SPNR	3.0	8V	-40 to 125°C	YES	9.9X3.9X1.75	SOP16	2	2500
NSI6602VB-Q1SPOR	3.0	8V	-40 to 125°C	YES	9.9X3.9X1.75	SOP14	2	2500
NSI6602VC-Q1SWR	5.7	13V	-40 to 125°C	YES	10.3X7.5X2.65	SOW16	2	1000
NSI6602VC-Q1SWKR	5.7	13V	-40 to 125°C	YES	10.3X7.5X2.65	SOW14	2	1000
NSI6602VC-Q1SPNR	3.0	13V	-40 to 125°C	YES	9.9X3.9X1.75	SOP16	2	2500
NSI6602VC-Q1SPOR	3.0	13V	-40 to 125°C	YES	9.9X3.9X1.75	SOP14	2	2500
NSI6602VD-Q1SWR	5.7	4V	-40 to 125°C	YES	10.3X7.5X2.65	SOW16	2	1000
NSI6602VD-Q1SWKR	5.7	4V	-40 to 125°C	YES	10.3X7.5X2.65	SOW14	2	1000
NSI6602VD-Q1SPNR	3.0	4V	-40 to 125°C	YES	9.9X3.9X1.75	SOP16	2	2500
NSI6602VD-Q1SPOR	3.0	4V	-40 to 125°C	YES	9.9X3.9X1.75	SOP14	2	2500

12. Tape and Reel Information

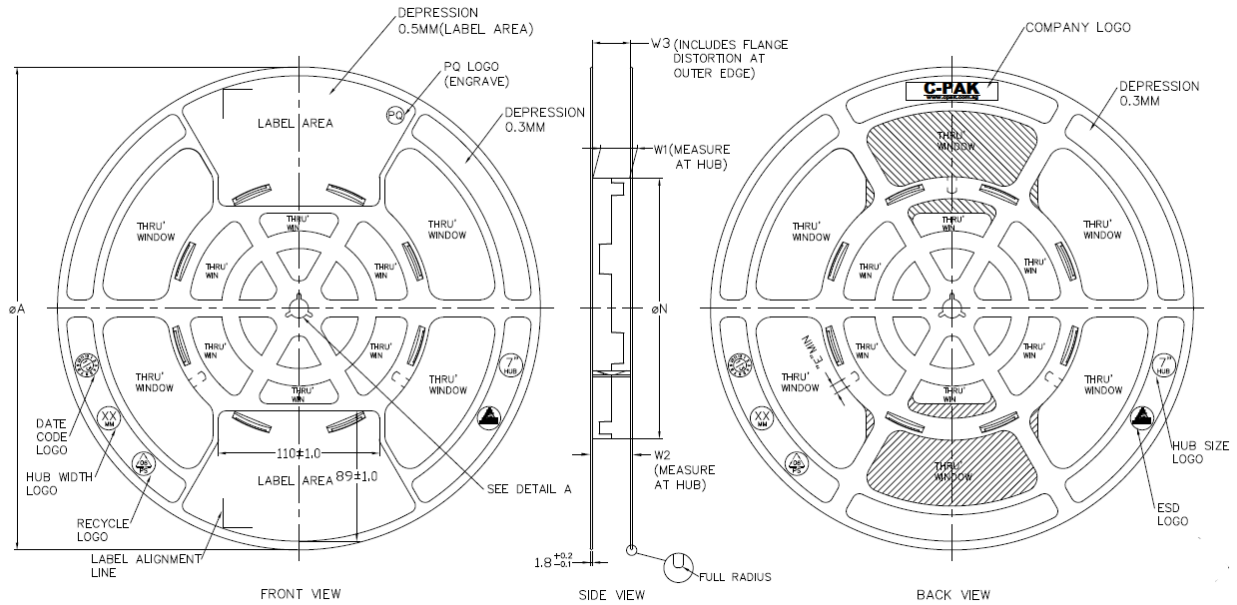
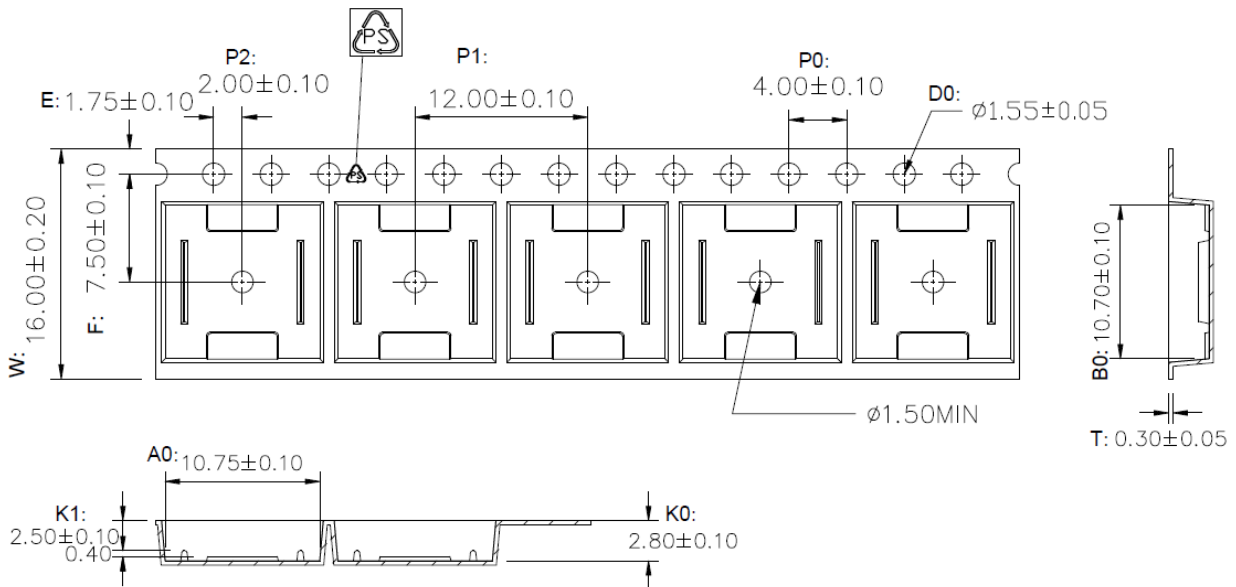


Figure 12.1 Tape Information



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 378 Meters.(N=122)
7. Component load per 13" reel : 1000 pcs.

Figure 12.2 SOW16/SOW14 Reel Information

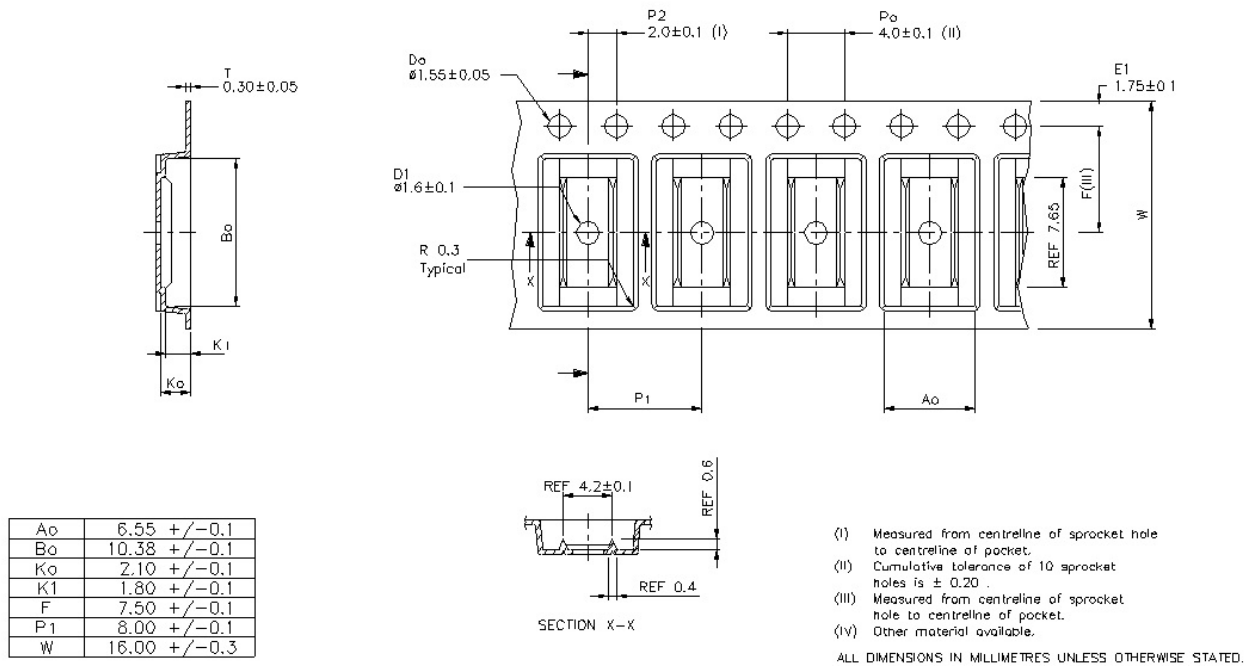


Figure 12.3 SOP16 Reel Information

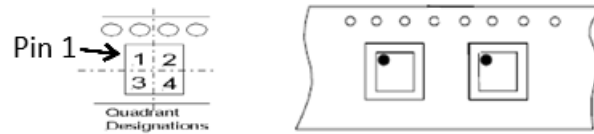


Figure 12.4 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
0.1	Initial version	2023/7/10

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